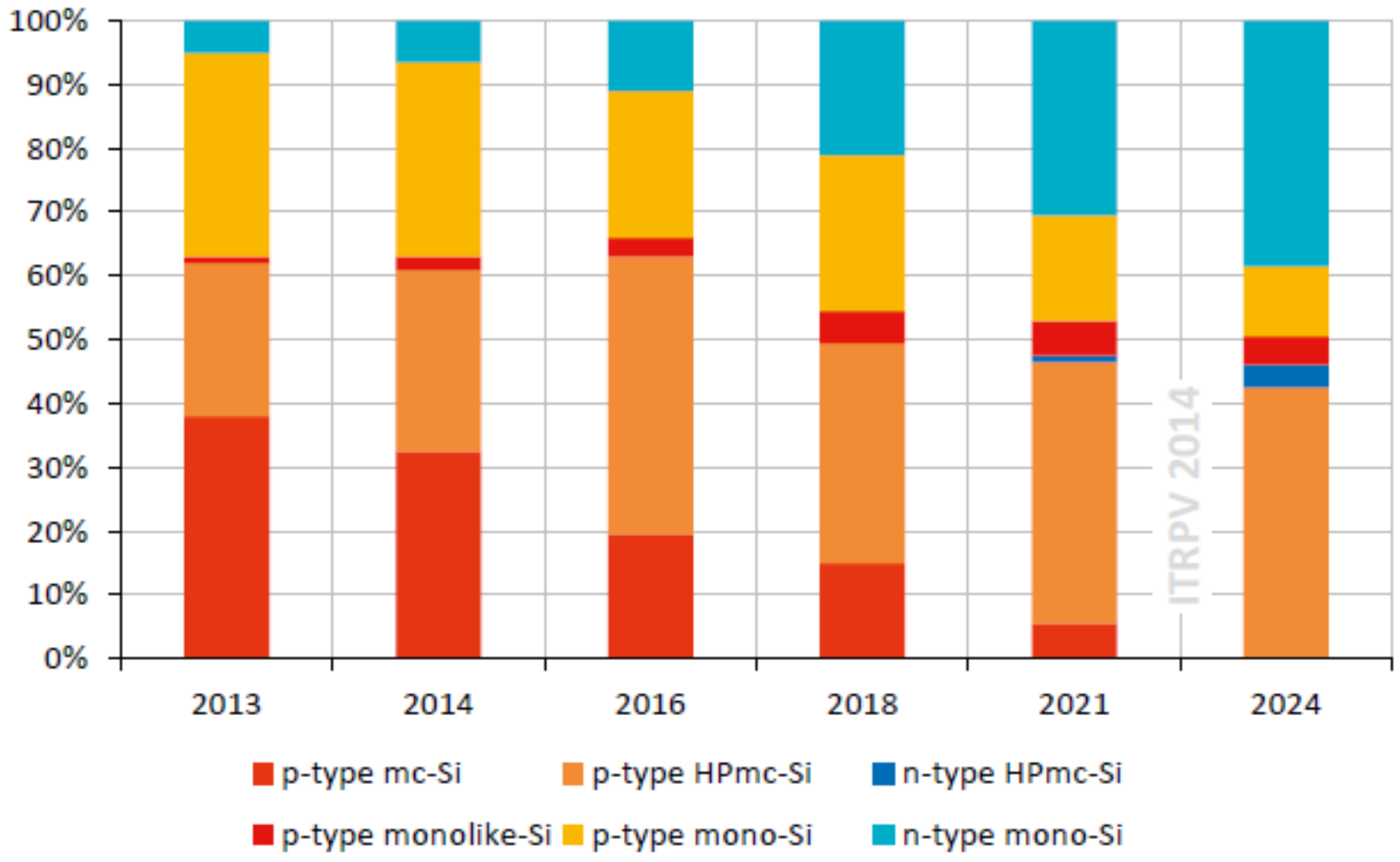
# Novel n-type wafer-based silicon solar cell architectures being developed at imec

**IMEC ENERGY**

Ivan Gordon

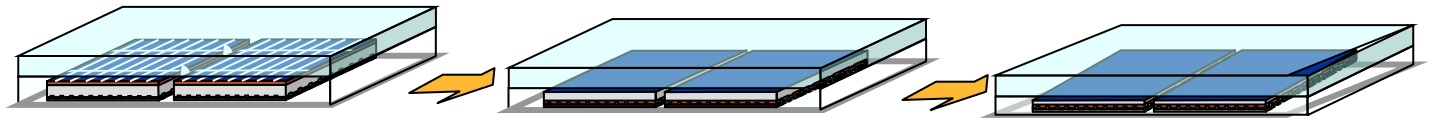
# THE MARKET SHARE OF N-TYPE DEVICES IS EXPECTED TO INCREASE SUBSTANTIALLY




http://www.itrpv.net/

# THE CURRENT IMEC Si-PV ROADMAP IS FOCUSED ON N-TYPE DEVICES

| 21-22.5 % | 23-25 % | 23-24 % |
|---|---|---|
| ” n-PERT” | i$^2$-BC” | “i$^x$-module” |
| ≥120 µm | ≥ 80 µm | ≥ 40 µm |



| Rear surface processing | Interdigitated back contacts | Transferred epi-foils and module level processing |
|---|---|---|

**High-efficiency n-PERT solar cells**

- 2-side contacted devices on 156x156 mm$^2$ n-type wafers

**High-efficiency IBC solar cells**

- Back-contact devices on 156x156 mm$^2$ n-type wafers

**I$^x$-module approach**

- Novel approach to process ultra-thin n-type Si-foils bonded on glass

# Affiliation Partners Si-PV

- Energy industry
- Solar cell producers
- Academia
- Materials suppliers
- Tool suppliers

TOTAL

kaneka

KYOCERA

Kuwait University

SoLayTec

RENA

TEMPRESS AMTECH GROUP

Meco

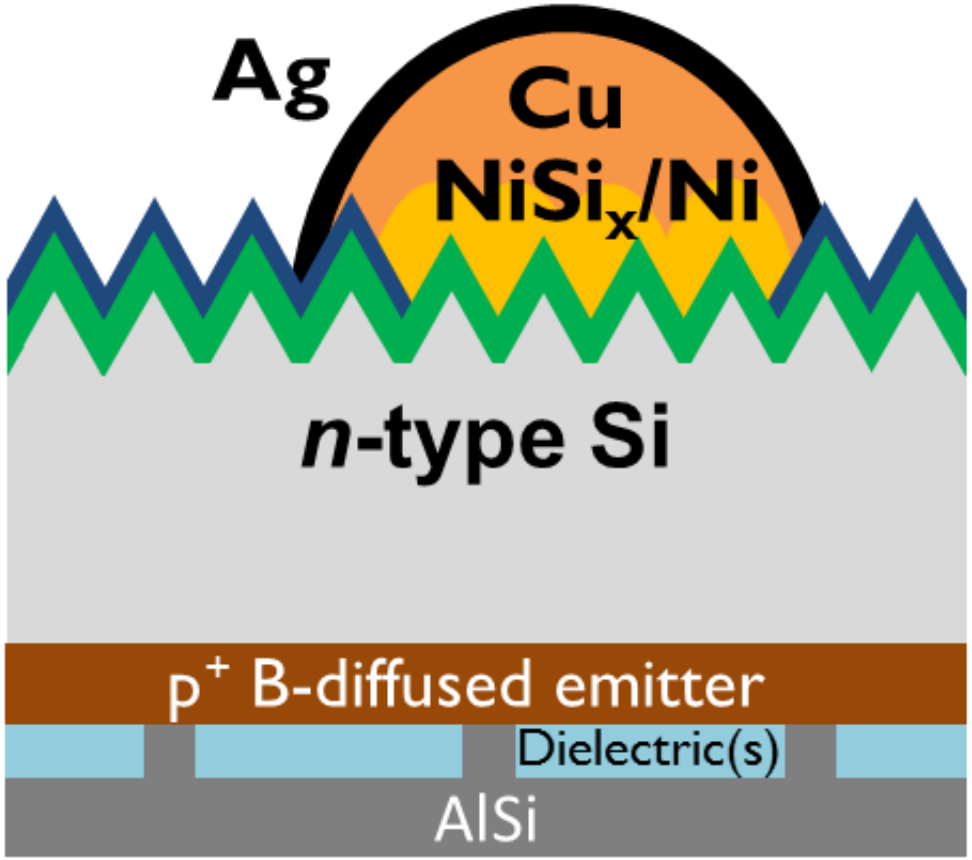
# OUTLINE

n-type PERT cells with Cu contacts

Interdigitated back contact cells

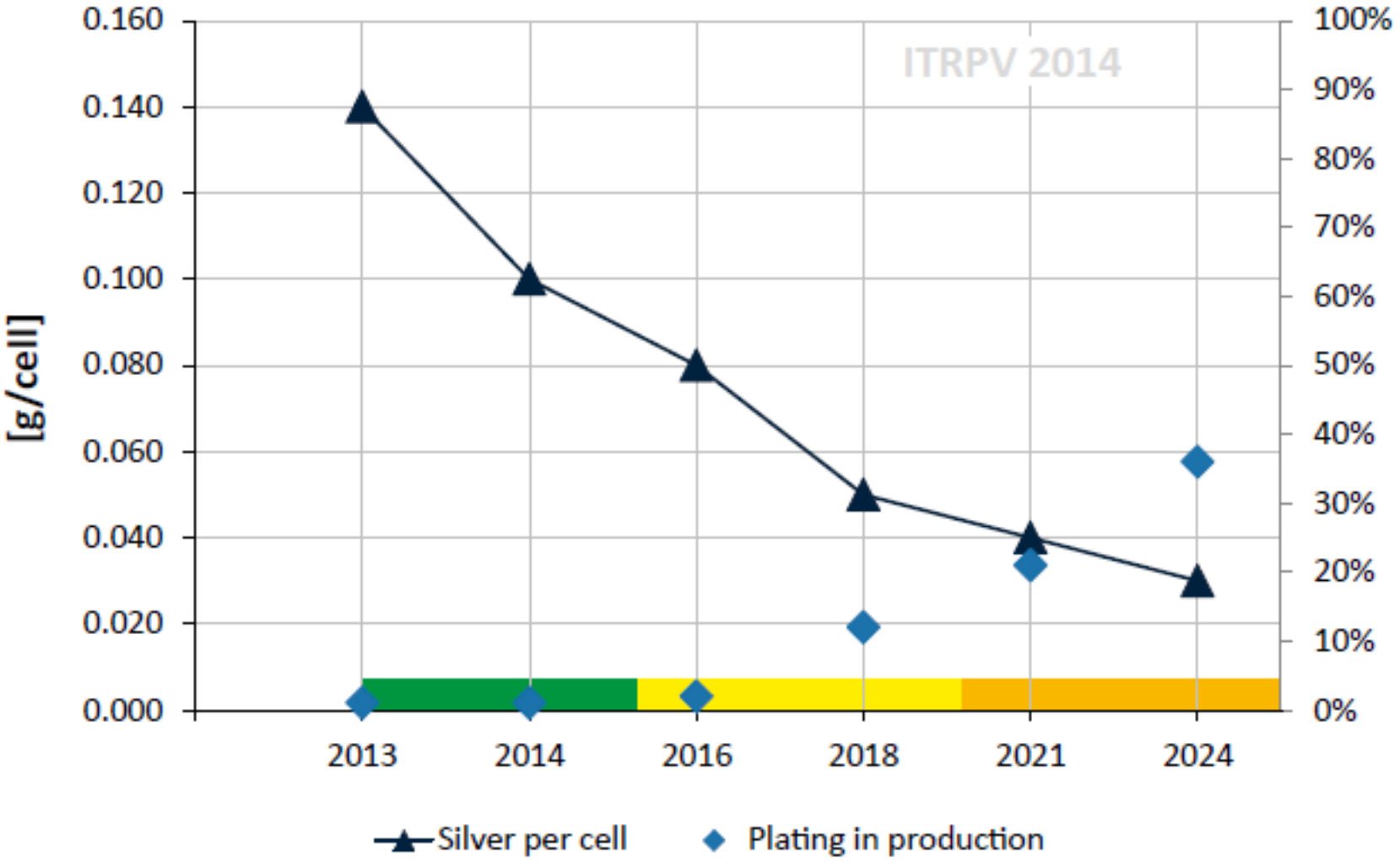
Module-level processing of epitaxial foils

# REAR EMITTER n-PERT DEVICE STRUCTURE



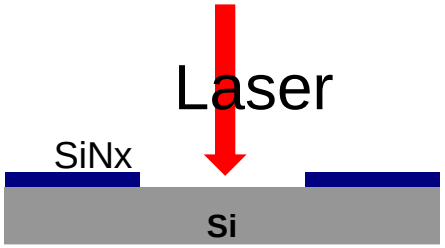

- n-type wafers
  - 6 inch Cz
  - 150-170 µm thick
- Front side
  - n+ FSF + $SiO_2/SiN_x$ stack
  - Ni/Cu plated contacts
- Rear side
  - p+ emitter: BBr3 diffusion
  - Dielectric passivation with local contacts

# THE AMOUNT OF Ag USED PER CELL NEEDS TO DECREASE SUBSTANTIALLY



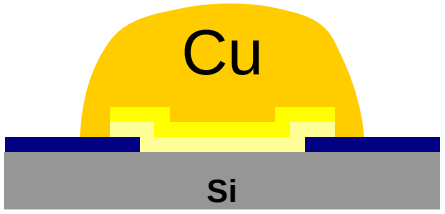

http://www.itrpv.net/

# IMEC FOCUSES ON REPLACING Ag SCREEN PRINTING BY Cu PLATING

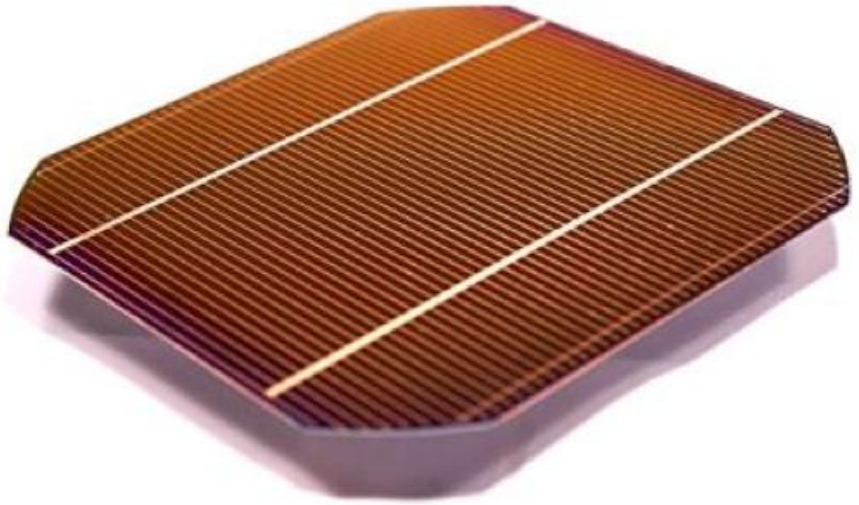



***LASER ABLATION***


***Ni EL-PLATING***




***Cu E-PLATING***



Cu metallisation can give you

- Cost reduction (Cu vs. Ag)
- Increased performance (lower resistance, less shadow losses, higher resistive diffused layers, ...)

Imec focuses on

- Cost effective and upscaleable processing
- Stability and reliability evaluation

# HIGH EFFICIENCIES CAN BE REACHED WITHOUT LIGHT-INDUCED DEGRADATION

Best devices obtained so far:

| | Jsc ($mA/cm^2$) | Voc (mV) | FF (%) | Eta (%) |
|---|---|---|---|---|
| Measured at ISE CalLab | 39.9 | 684 | 80.7 | **22.0** |

*Front : Selective FSF by laser doping*
*Rear : ALD Al2O3 surface passivation*

*Area = 226$cm^2$*

No light induced degradation in n-type cells

| As processed | Jsc ($mA/cm^2$) | Voc (mV) | FF (%) | Eta (%) |
|---|---|---|---|---|
| p-type PERC | 39.4 | 662 | 78.6 | 20.5 |
| n-type PERT | 39.4 | 676 | 80.2 | **21.4** |

| After 12h light soaking at 1 sun | Jsc ($mA/cm^2$) | Voc (mV) | FF (%) | Eta (%) |
|---|---|---|---|---|
| p-type PERC | 39.3 | 659 | 76.6 | 19.8 |
| n-type PERT | 39.4 | 675 | 80.3 | **21.4** |

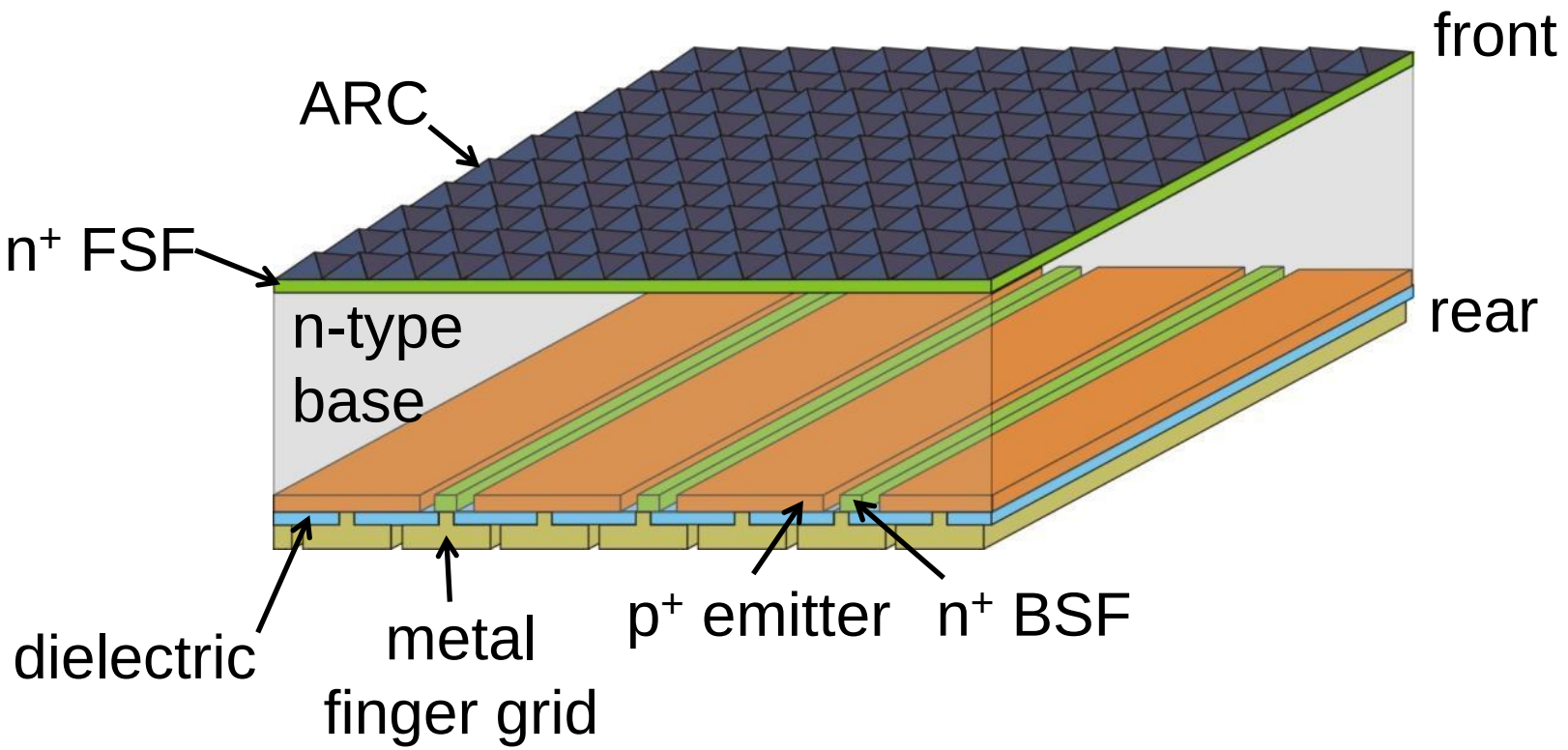
# OUTLINE

n-type PERT cells with Cu contacts

Interdigitated back contact cells

Module-level processing of epitaxial foils

# INTERDIGITATED BACK CONTACT SILICON SOLAR CELLS



# IBC: STATE-OF-THE-ART

Industrial and semi-industrial homo-junction IBC cells

| Reference | Year | Substrate | Area ($cm^2$) | Eff. (%) |
|---|---|---|---|---|
| [1] D. Smith, SunPower | 2014 | CZ, n-type | 155 | 24.5 |
| [1] D. Smith, SunPower | 2014 | CZ, n-type | 121 | 25.0 |
| [2] C.B. Mo, Samsung SDI/Varian | 2012 | CZ, n-type | 155 | 22.4 |
| [3] A. Halm / J. Libal, ISC Konstanz / Silfab | 2012 | CZ, n-type | 243 | 21.3 |
| [4] Bosch / ISFH | 2013 | CZ, n-type | ~240 | 22.1 |
| [5] E. Franklin, ANU/Trina Solar | 2014 | CZ, n-type | ~240 | 22.9 |

[1] D. Smith et al., 40th IEEE PVSC, Denver, USA (2014)

[2] C.B. Mo et al., 27nd EUPVSEC, Frankfurt, Germany (2012)

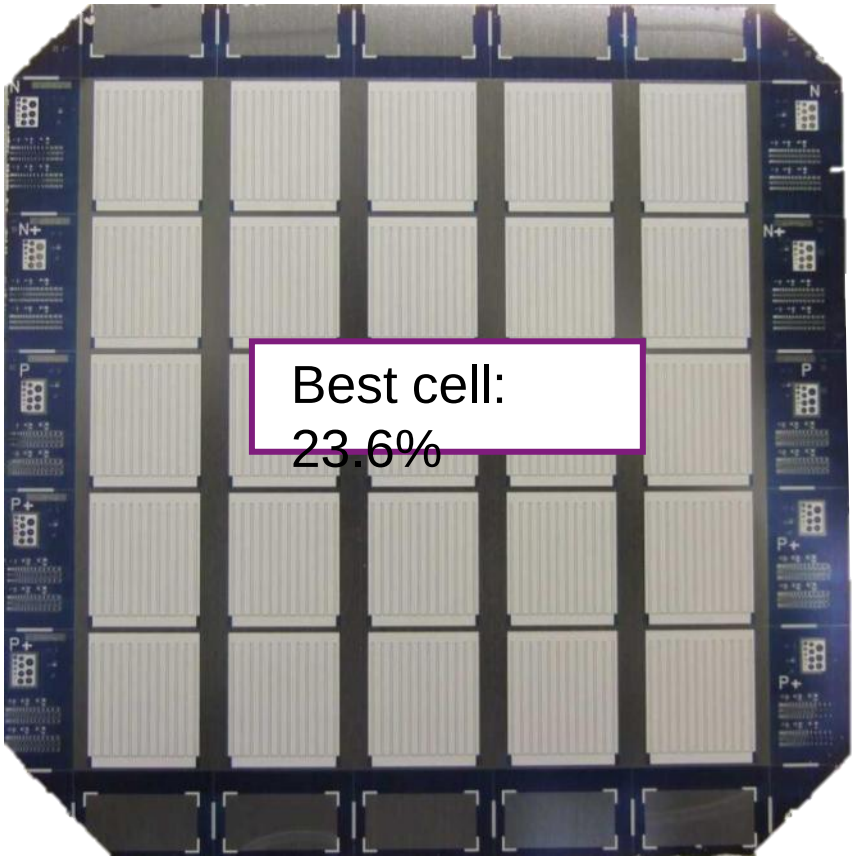
[3] A. Halm et al., 27nd EUPVSEC, Frankfurt, Germany (2012)

[4] Bosch SE, press release (2013)

[5] E. Franklin et al., SNEC, Shanghai, China (2014)

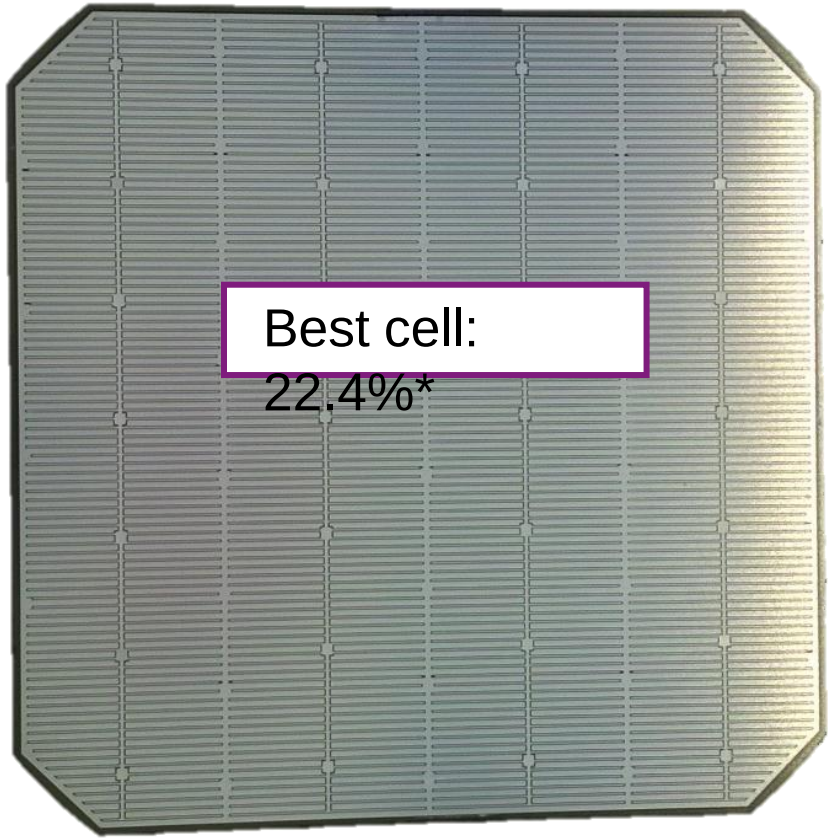
# SMALL AREA IBC CELLS

- Wafers:
  - 15.6x15.6 cm2 semi-square
  - n-type Cz
  - Commercially available
- Processing:
  - Doping: diffusion
  - Patterning: photolithography
- Layout:
  - 25 cells with an active area of 2x2 $cm^2$
  - 5 different designs with different contact fractions for BSF and emitter



# LARGE AREA IBC CELLS

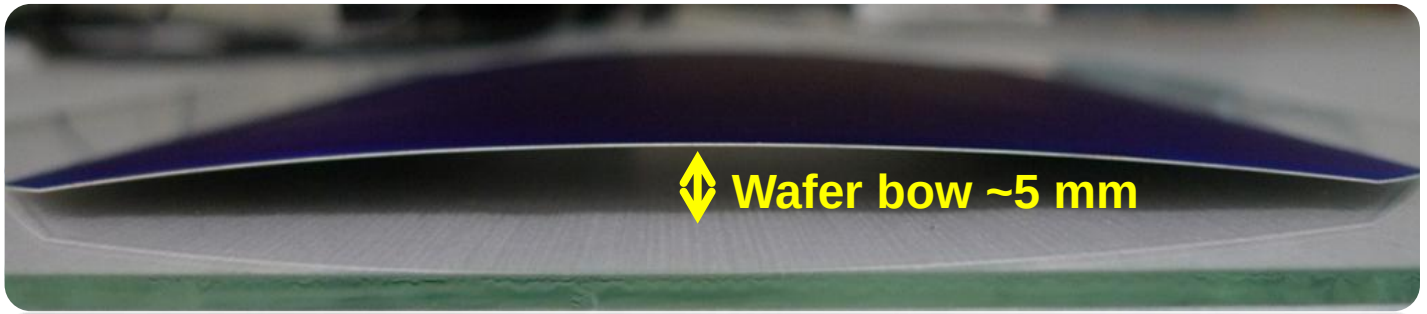
- Wafers:
  - 15.6x15.6 $cm^2$ semi-square
  - n-type Cz
  - Commercially available
- Processing:
  - Doping: diffusion
  - Patterning: laser ablation and screen printing
- Cells:
  - One cell
  - 5 emitter busbars with 8 solder points on each busbar
  - 4 BSF busbars with 7 solder points on each busbar




* 227 $cm^2$

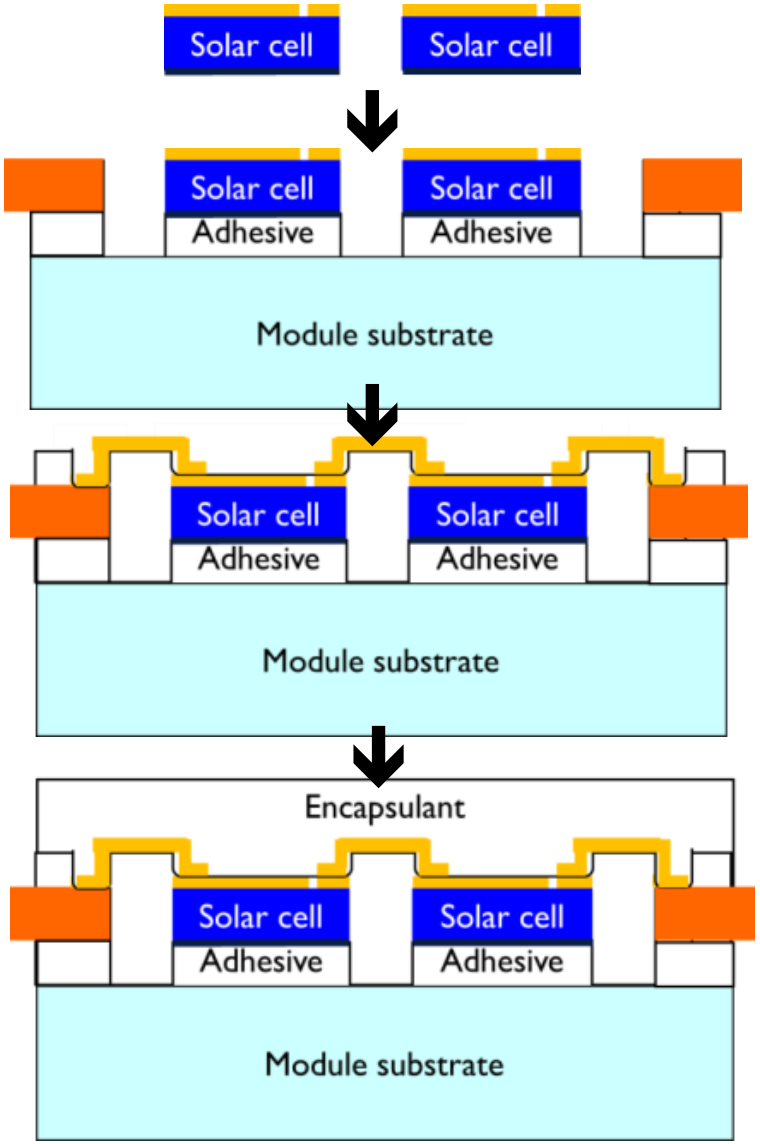
# IBC CELLS ARE SLIGHTLY BOWED

- Cu-plated metallization used(1-sided)
- Ag-plated capping for soldering




- Module processing: Bonding before interconnection to support (thin and/or curved) cells during interconnection

# ENVISAGED INTERCONNECTION FLOW




➔ Start from finished (BC) cells

IBC

➔ Bonding to glass (superstrate)

Silicone coating
Placement

➔ Interconnection

Soldering/tabbing

➔ Encapsulation

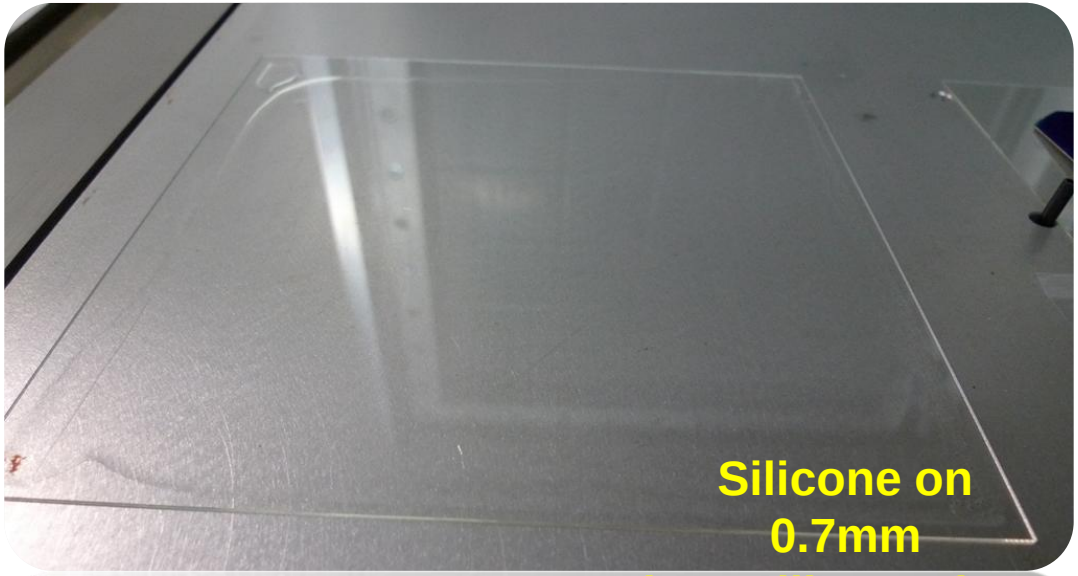
Silicone encapsulation
+ back sheet lamination

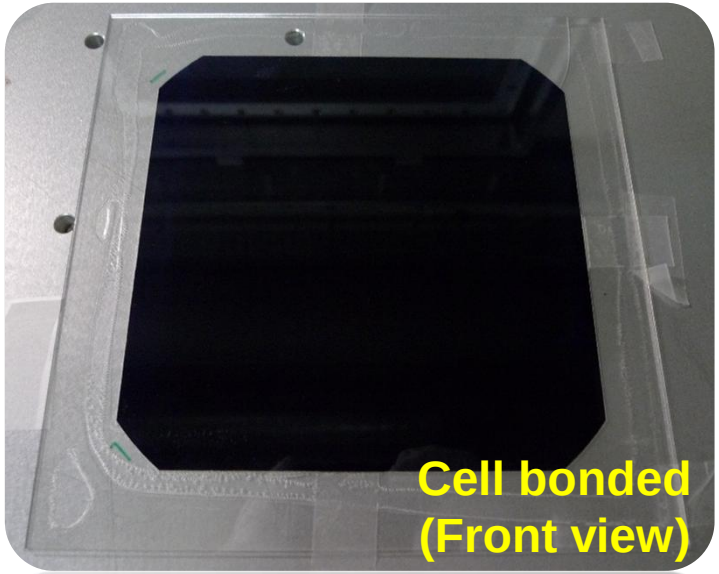
# ONE-CELL LAMINATE DEMONSTRATOR

# CELL IS FIRST BONDED TO GLASS

## Silicone bonding

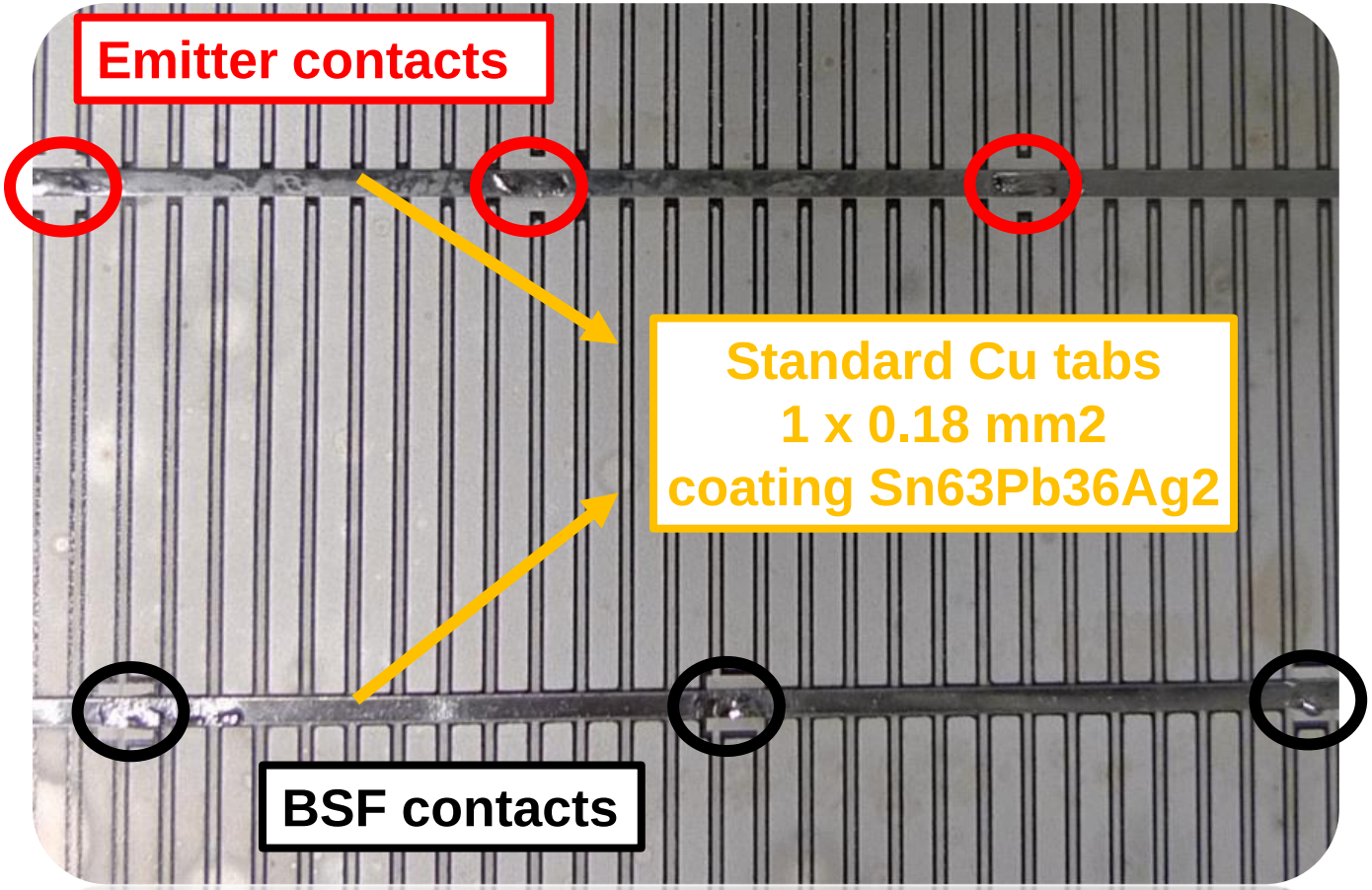
- Single layer coating on glass + curing (15 min @ 100˚C)
  (“hybrid” stencil printing / blade coating)
- Alignment, placement, bonding (vacuum laminator)



# INTERCONNECTION TABS ARE THEN APPLIED

Soldering/tabbing process (manual)

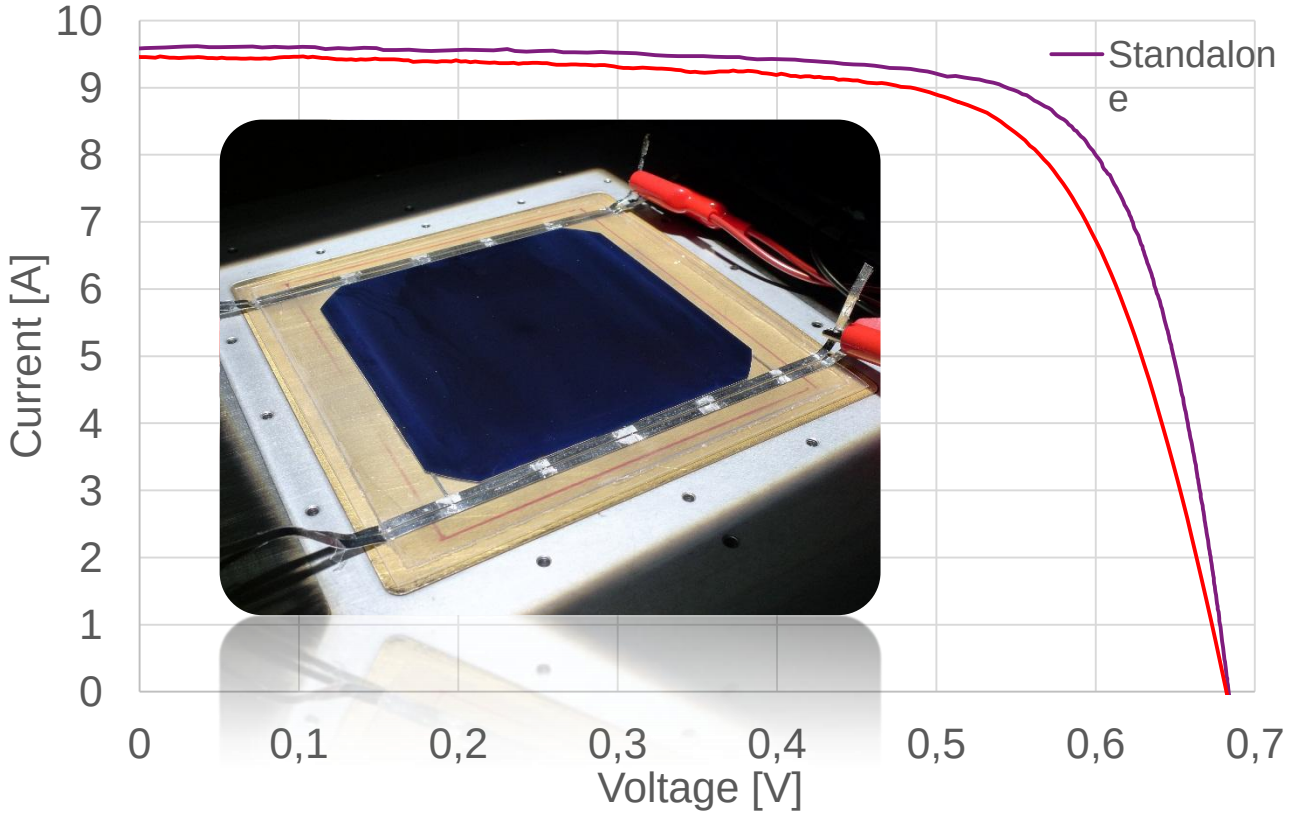


# FINALLY, THE DEVICE IS ENCAPSULATED

Silicone coating + lamination

- Dispensing of silicones
- Placement of transparent back sheet
- Lamination cycle ~6 min @ 110˚C

# RESULTS




| | $J_{sc}$ [mA/cm²] | $V_{oc}$ [mV] | FF [%] | Eta [%] |
|---|---|---|---|---|
| Standalone cell | 40.1 | 684 | 75.5 | 20.7 |
| Laminate | 39.6 | 682 | 71.2 | 19.2 |

# RESULTS

| | $J_{sc}$ [mA/cm$^2$] | $V_{oc}$ [mV] | FF [%] | η [%] |
|---|---|---|---|---|
| Standalone cell | 40.1 | 684 | 75.5 | 20.7 |
| One-cell laminate | 39.6 | 682 | 71.2 | 19.2 |

$J_{sc}$ drop caused by increased reflection at the glass/air interface

FF drop caused by narrow tabs (0.18x1 mm$^2$)

Can be tackled by more advanced module technologies for IBC cells

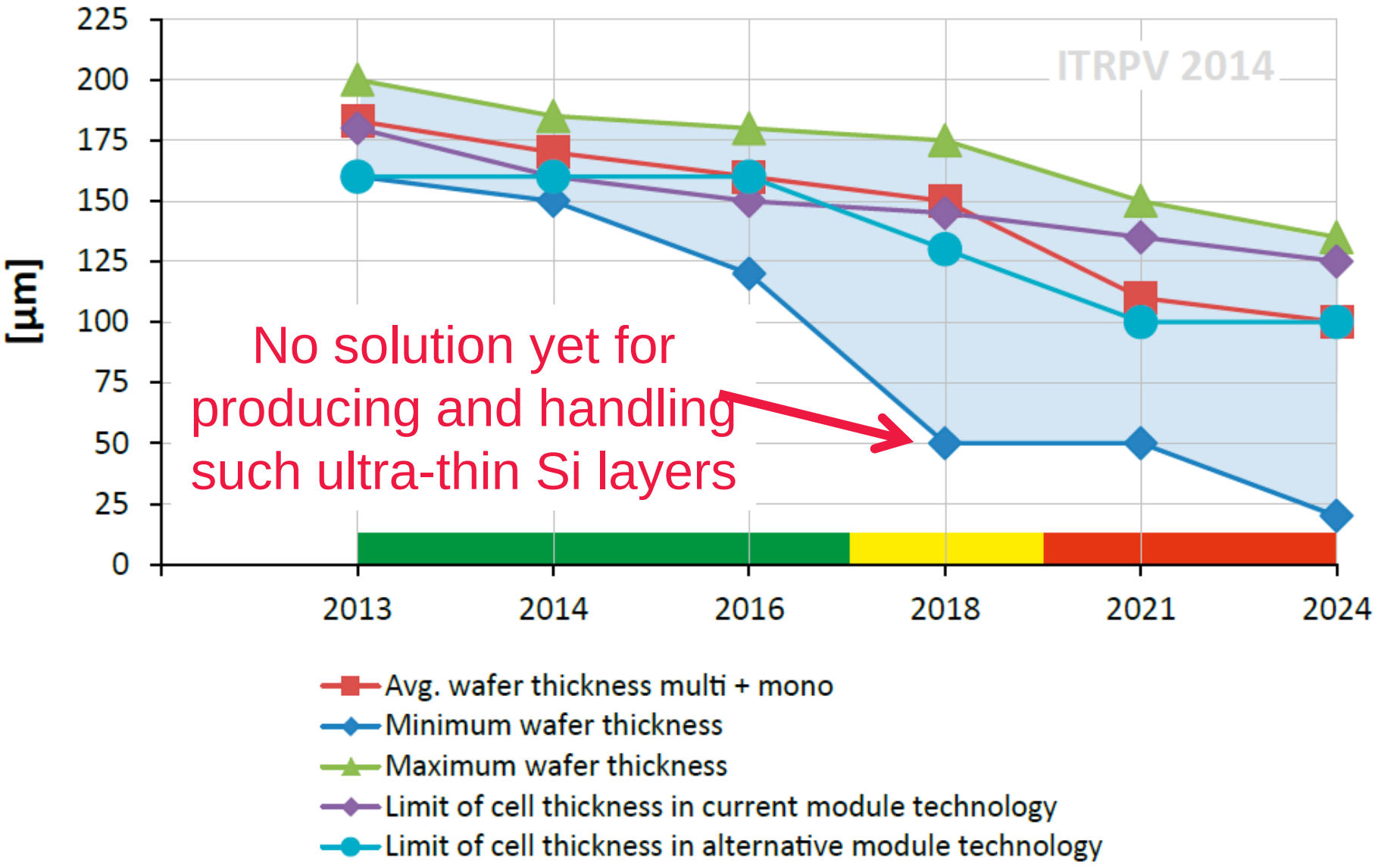
# OUTLINE

n-type PERT cells with Cu contacts

Interdigitated back contact cells

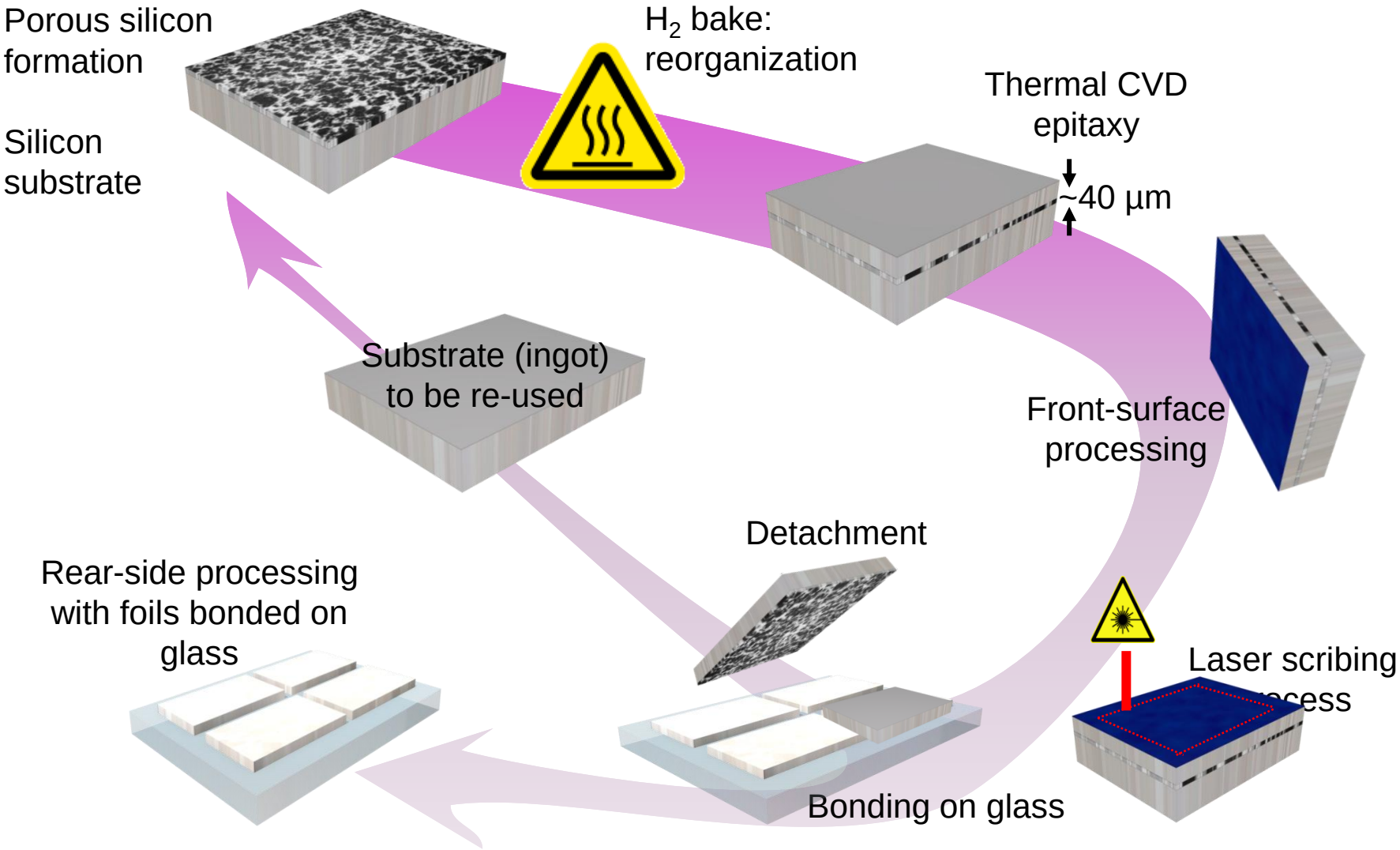
Module-level processing of epitaxial foils

# REDUCING COST BY REDUCING Si THICKNESS

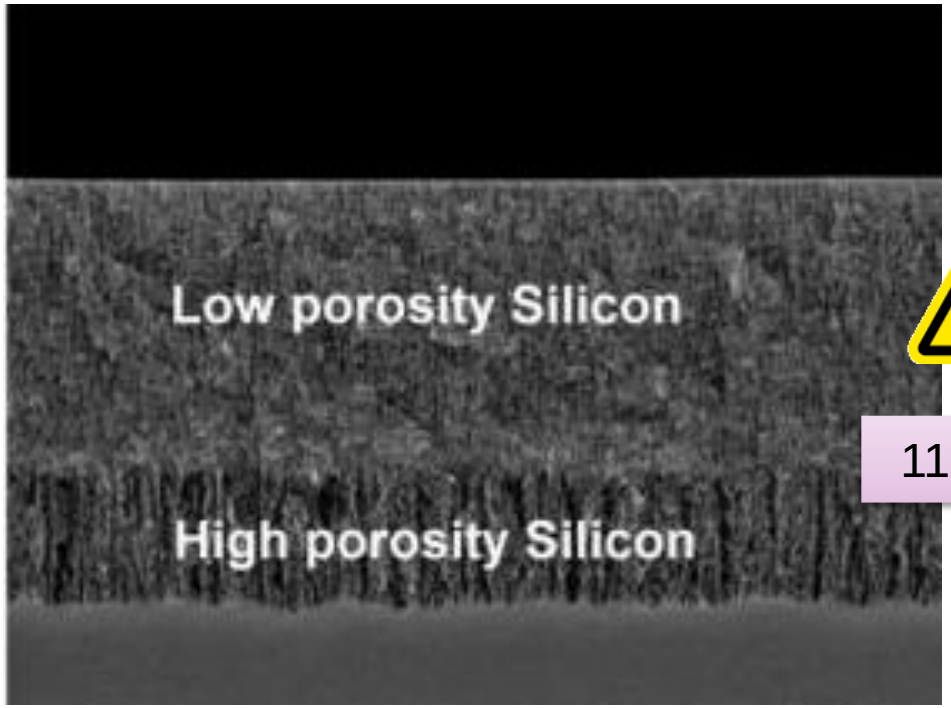



http://www.itrpv.net/

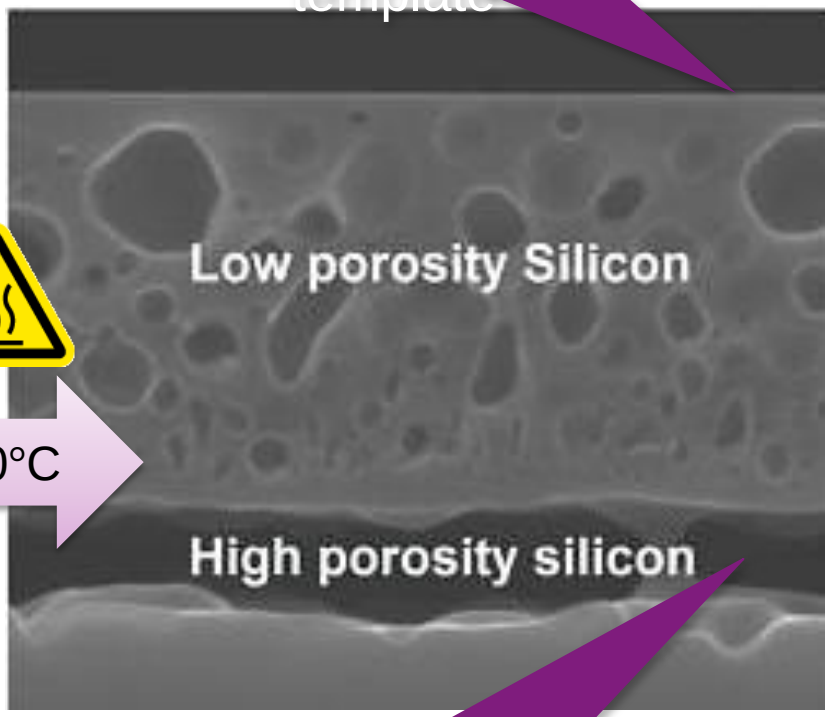
# IMEC'S APPROACH: FROM EPITAXIAL SILICON FOILS TO DEVICES ON GLASS



# POROUS SILICON SERVES AS TEMPLATE FOR EPITAXY AND AS DETACHMENT LAYER




1130°C

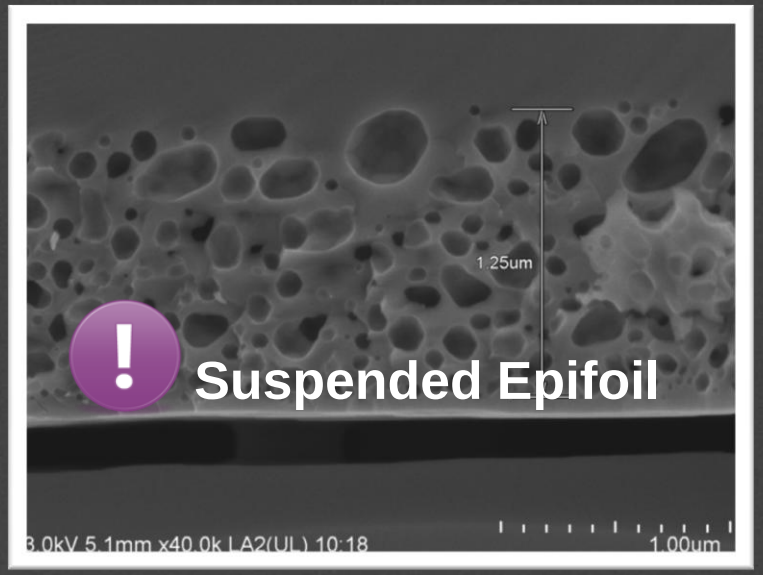



Closed smooth surface acting as epitaxy template

After electrochemical etching

Continuous void acting as detachment layer

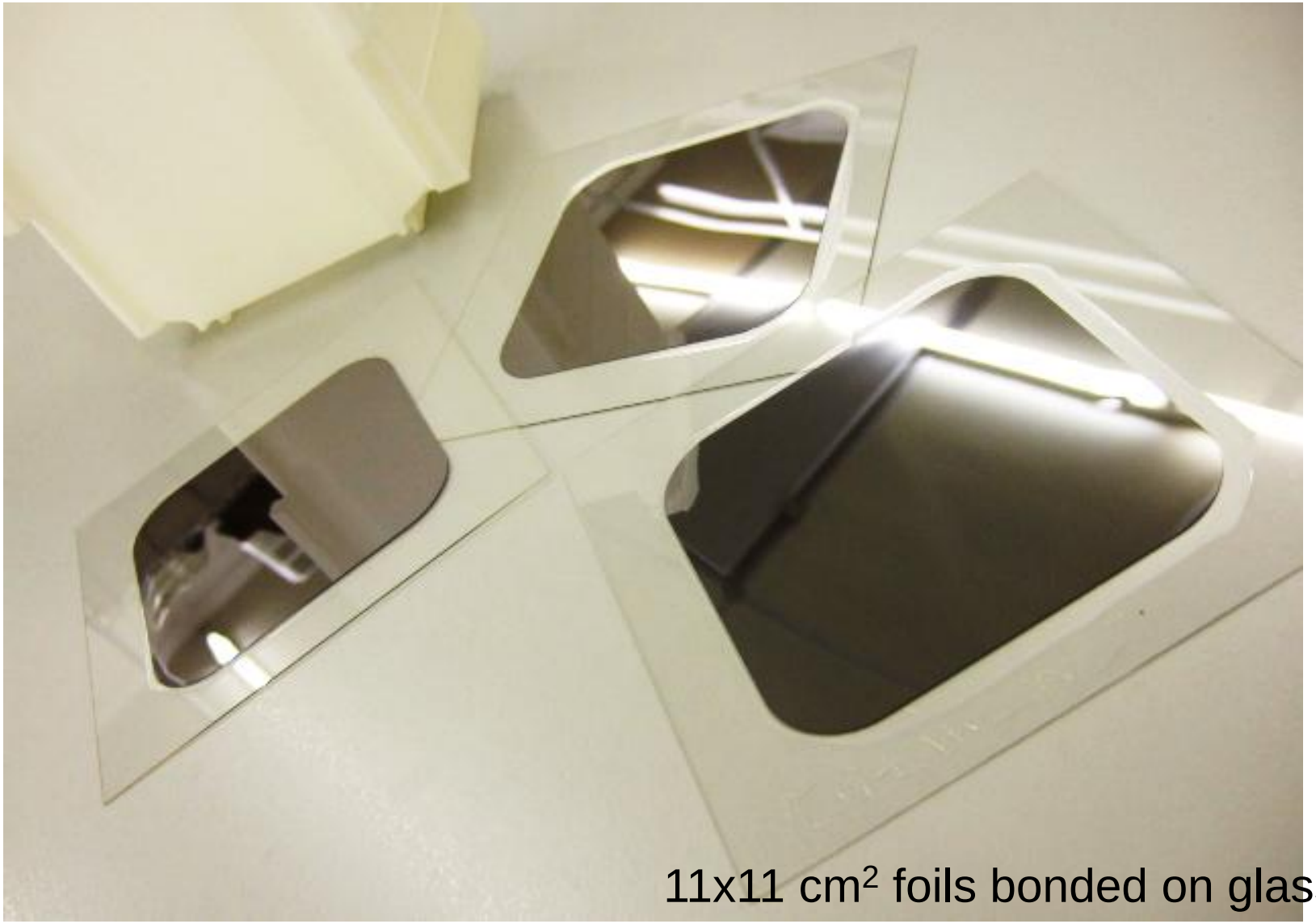
**Epifoil** – 40 µm, n-type




**High-porosity layer** – 300 nm

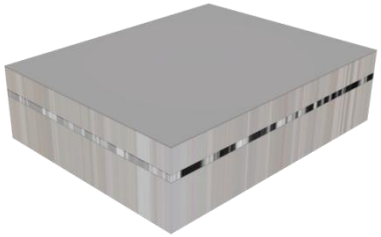
**Parent substrate** – 725 µm

# 11X11CM$^2$ FOILS ARE ROUTINELY DETACHED

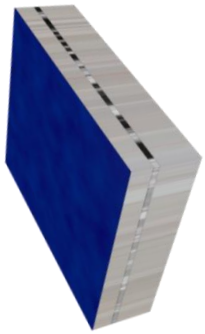


11x11 cm$^2$ foils bonded on glass

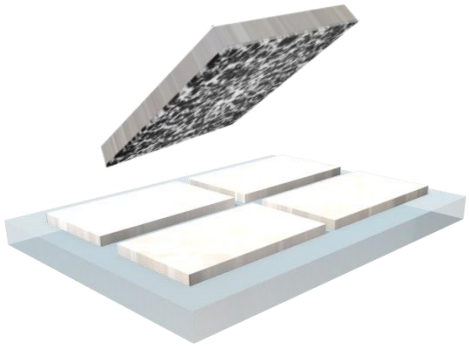
# FROM EPITAXIAL SILICON FOILS TO DEVICES ON GLASS



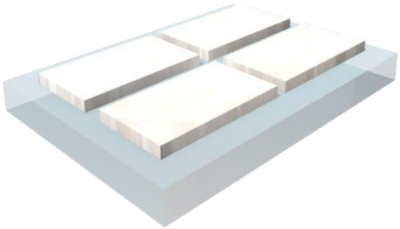
Thermal CVD epitaxy



Front-surface processing

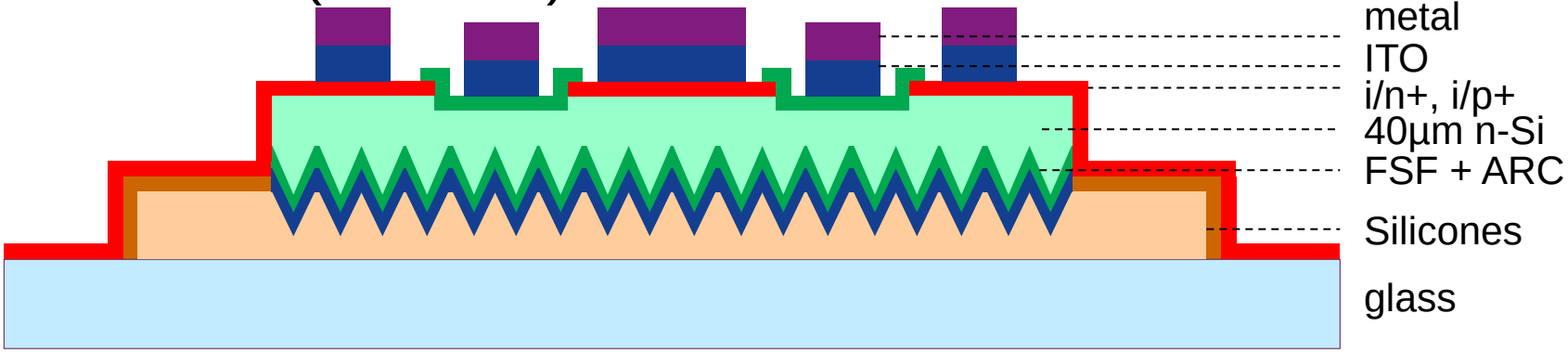


Detachment and bonding on glass

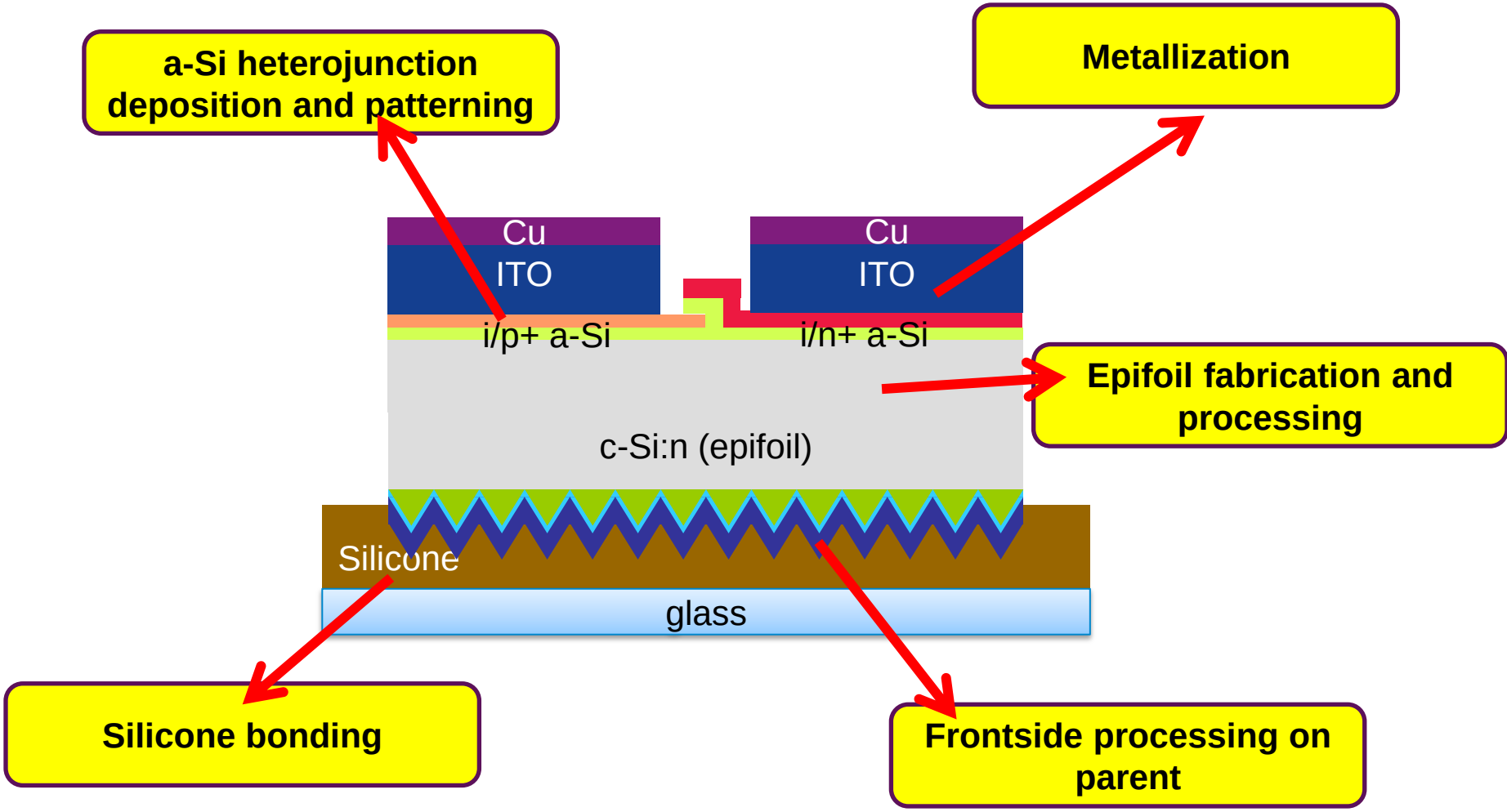


Rear-side processing with foils bonded on glass

Targeted cell structure based on a-Si heterojunction and back contacts (HJT-IBC)



# DEVICE INTEGRATION




At device level: first simple devices of epifoils bonded to glass using silicones: **Voc values ~ 695 mV**

# SUMMARY

- World-class n-PERT cells of 22.0% efficiency are made using Cu-plated front contacts

- Large-area IBC cells require novel interconnection and encapsulation processes

- We are working towards the processing of ultra-thin foils into working devices directly at module level

Acknowledgements:

All members of imec's PV department

Imec's Industrial Affiliation Programme

EU-FP7 projects "Cheetah" and "Cu-PV"